REMARKS

In the Office Action, the Examiner rejected Claims 1, 3, 5-8, 11-13, 15-19 and 21 under 35 U.S.C. 103 as being unpatentable over the prior art. Claim 10 was allowed, and the Examiner objected to Claim 20 and indicated that Claim 20 would be allowable if appropriately rewritten.

With regard to the rejection of the claims over the prior art, Claims 1, 3, 5, 11-13, 15-17 and 21 were rejected as being unpatentable over U.S. Patent 5,880,983 (Elliott, et al.) in view of U.S. Patent 6,480,872 (Choquette), and Claims 6-8, 18 and 19 were rejected as being unpatentable over Elliott, et al. in view of Choquette and further in view of U.S. Patent 7,228,325 (Willson, Jr. et al.).

It is noted that the previous rejection of the claims based on the combination of Elliott, et al. and U.S. Patent Application Publication No. 2004/0122886 (Gerwig, et al.) was withdrawn.

Amendments are being made to independent Claims 1 and 13 to improve the readability of these claims. Claims 3, 5, 15, 16 and 17 are being cancelled to reduce the number of issues in this application, and Claim 11 is being amended to be dependent from Claim 1, instead of the now cancelled Claim 3. Also, new Claims 22 and 23, which are dependent from Claim 1, are being added to describe features of an embodiment of the invention.

For the reasons advanced below, Claims 1, 6-8, 11-13 and 18-23 patentably distinguish over the prior art and are allowable. The Examiner is thus respectfully asked to reconsider and to withdraw the rejection of Claims 1, 6-8, 11-13, 18, 19 and 21-23 under 35 U.S.C. 103 and the objection to Claim 20, and to allow Claims 1, 6-8, 11-13 and 18-23.

Generally, Claims 1, 6-8, 11-13 and 18-23 patentably distinguish over the prior art because the prior art does not disclose or render obvious the way in which the shift calculation is performed, as described in independent Claims 1 and 13. More specifically, the prior art does

not disclose or render obvious calculating that shift amount based on the exponent of the same operand that is selected to be sent to the aligner, as described in independent Claims 1 and 13.

The present invention, generally, relates to a high speed floating point execution unit. As discussed in the instant application, high speed data processing systems typically are provided with high-seed floating point units (FPUs) that perform floating poi8nt operations such as add, subtract and multiply. These systems typically utilize a pipelined architecture, providing for a multistage data flow.

In operation, an FPU unpacks the operands from a packed floating point format – that is, the FPU extracts the sign, exponent and mantissa from the packed format. This unpacking cal slow down the execution of the FPU.

In an embodiment, the present invention removes the operand formatting/selection and unpacking step from the timing critical path of an FPU, increasing the performance of the FPU significantly.

More specifically, an embodiment of the invention is a floating point execution unit for performing multiply/add operations on a floating point number comprising a plurality of operands taken from an instruction having a plurality of floating point number operand positions. This FPU comprises a multiplier for calculating a product of two of the operands; and a first data path for supplying to the multiplier the first and second operands from the instruction. The multiplier multiplies these two operands to produce a product operand.

The FPU also comprises an aligner, and a second data path for supplying one of the operands from the instruction to the aligner. In particular, a multiplexer is on the second data path for receiving the second and third operands from the instruction, for selecting one of these two operands, and sending the selected one of the operands to the aligner.

The FPU further comprises a shift calculator for determining a shift amount for this selected one of the operands. This shift calculator, shown in Figure 5 of the application and discussed on page 8, includes a first unit for calculating a shift component using exponents of the first and second operands, and a second unit for calculating this shift amount using this shift component and the exponent of the above-mentioned selected one of the operands. In an embodiment, a multiplexer is provided for receiving exponents of the second and third operands, and for sending to the second unit of the shift calculator the exponent of the selected one of the operands.

The aligner shifts the selected one of the operands the shift amount to generate a shifted operand. An adder is used for adding the product operand from the multiplexer and this shifted operand to produce a result.

With the above-procedure, the first data path, which supplies the operands to the multiplier, is kept free of multiplexer operations. This, in turn, helps to increase the speed of operation of the FPU.

The prior art does not disclose or render obvious the above-described shift calculator and the way this calculator determines the shift amount.

For example, Elliot, et al. discloses a floating point unit having split multiply/add systems. In this FPU, a multiplier multiplies a firs portion of a plurality of operands to provide a product, and an adder combines this product and a remaining portion of the plurality of operands. The adder includes at least one pair of data paths. A first of these data paths comprises a first aligner, a first adder, and a first normalizer for shifting a mantissa; and the second data path, similarly, comprises a second aligner, a second adder, and a second normalizer for shifting a mantissa.

Choquette describes a floating point unit that can be configured to perform a floating-point multiply-add or an integer multiply-accumulation in response to control signals. This reference was cited primarily for its disclosure of an aligner directly coupled to the multiplier.

There is no disclosure, however, in either Elliot, et al. or Choquette of calculating the shift amount the way in which it is calculated in Applicants' invention – that is, calculating that shift amount based on the exponent of the same operand that is selected to be sent to the aligner.

This feature is of utility because it shifts the multiplexing operations out of the data path to the multiplier and into the data paths leading to the aligner and the shift calculator. As explained in the present application, this increases the speed of Applicants' FPU.

Independent Claims 1 and 13 are being amended to describe this feature of the present invention. Specifically, these claims are being amended to describe a multiplexer on the second data path, leading to the aligner, for selecting one of the second and third operands and sending that selected one of the operands to the aligner. Claims 1 and 13, as presented herewith, also describe determining a shift amount for the selected operand based on a shift component calculated from exponents of the first and second operands, and the exponent of the above-mentioned selected one of the operands.

The other references of record have been reviewed, and these other references, whether considered individually or in combination, also do not disclose or render obvious this feature of the present invention.

For example, Wilson, Jr. et al. describes an adder having a bypass input and a logic circuit to hold one of two inputs as determined by an input applied to the bypass input. Here too, there is no teaching, disclosure or suggestion of calculating the shift amount for a floating point unit as is done in Applicants' invention.

In view of the above-discussed differences between Claims 1 and 13 and the prior art, and because of the advantages associated with those differences, Claims 1 and 13 patentably distinguish over the prior art and are allowable. Claims 6-8, 12 and 21-23 are dependent from Claim 1 and are allowable therewith. Likewise, Claims 18-20 are dependent from, and are allowable with, Claim 13. The Examiner is, accordingly, respectfully requested to reconsider and to withdraw the rejection of Claims 1, 6-8, 11-13, 18, 19 and 21-23 under 35 U.S.C. 103 and the objection to Claim 20, and to allow Claims 1, 6-8, 11-13 and 18-23.

For the reasons discussed above, it is believed that the present application is in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,

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